

ABSTRACT OF THE DISCLOSURE

Sub
A2
A memory data access structure and an access method suitable for use in a processor. For each instruction executed by the processor, the execution results are recognized by the processor and transferred to a cache memory via control signals.

- 5 When the instruction to be fetched is not stored in the cache memory, according to the control signals, the cache memory can determine whether the instruction is to be fetched from an external memory. With such structure, no matter whether the processor comprises a branch prediction mechanism or not, many operation clock cycles consumed in the processor of the prior art are saved by compensating for the situation that the cache
- 10 memory fails to fetch, that is, a Miss of the cache memory. The efficiency and performance of the processor can be effectively enhanced.

006221 2212560